Amendments to the Specification

Please amend the table on page 1 of the disclosure as follows:

Docket #	Serial #	Title
CNTR:2021	09/849736	SPECULATIVE BRANCH TARGET ADDRESS CACHE
CNTR:2022	09/849658	APPARATUS, SYSTEM AND METHOD FOR DETECTING AND CORRECTING ERRONEOUS SPECULATIVE BRANCH TARGET ADDRESS CACHE BRANCHES
CNTR:2023	09/849734	SPECULATIVE HYBRID BRANCH DIRECTION PREDICTOR
CNTR:2050	09/849822	DUAL CALL/RETURN STACK BRANCH PREDICTION SYSTEM
CNTR:2052	09/849799	SPECULATIVE BRANCH TARGET ADDRESS CACHE WITH SELECTIVE OVERRIDE BY SECONDARY PREDICTOR BASED ON BRANCH INSTRUCTION TYPE
CNTR:2063	09/849800	APPARATUS AND METHOD FOR TARGET ADDRESS REPLACEMENT IN SPECULATIVE BRANCH TARGET ADDRESS CACHE

Please replace the SUMMARY, which begins at page 14, with the following:

SUMMARY OF THE INVENTION

The present invention provides a branch target address cache that provides more efficient branch prediction by making a prediction for a plurality of branch instructions in a cache line. Accordingly, in attainment of the aforementioned object, it is a feature of the present invention to provide a pipelined microprocessor. The microprocessor includes an instruction cache that receives a fetch address on an address bus. The microprocessor also includes a branch target address cache (BTAC), coupled to the address bus, which provides a plurality of cached target addresses, offsets, direction predictions, and valid indicators indexed by the fetch address. Each of the plurality of cached target addresses, offsets, direction predictions, and valid indicators is associated with one of a plurality of previously executed branch instructions. Each of the plurality of offsets specifies a location of the associated previously executed branch instruction within a line of the

instruction cache selected by the fetch address. Each of the plurality of direction predictions predicts whether the associated branch instruction will be taken or not taken. Each of the plurality of valid indicators indicates whether the associated target address is a valid target address. The microprocessor also includes branch control logic, coupled to the BTAC, which generates a selector signal in response to the fetch address and the plurality of offsets, direction predictions, and valid indicators. The selector signal selects one of the plurality of target addresses provided by the BTAC as a subsequent fetch address on the address bus. The selector signal is used to select the one of the plurality of target addresses only if the associated valid indicator indicates that the target address is valid, only if the associated direction prediction predicts that the associated branch instruction will be taken, and only if the associated offset is greater than or equal to a predetermined plurality of least significant bits of the fetch address. If a plurality of the plurality of offsets is valid, taken, and greater than or equal to the portion of the fetch address, the selector signal is used to select the one of the plurality of target addresses whose associated offset is a smallest of the plurality of the plurality of valid, taken offsets greater than or equal to the portion of the fetch address.

In another aspect, it is a feature of the present invention to provide an apparatus for selecting a target address for one of a plurality of previously executed branch instructions, the plurality of previously executed branch instructions being potentially present in a line of an instruction cache selected by a fetch address, the fetch address provided to the instruction cache on an address bus. The apparatus includes a branch target address cache (BTAC), coupled to the address bus, which provides a plurality of target addresses cached therein indexed by the fetch address. The BTAC also provides a corresponding plurality of offsets within the instruction cache line for each of the plurality of previously executed branch instructions. The apparatus also includes control logic, coupled to the BTAC, which generates a selector in response to the fetch address and the offsets. The selector selects one of the plurality of target addresses. The control logic generates the selector to select the one of the plurality of target addresses that has a smallest one of the corresponding plurality of offsets greater than or equal to a corresponding portion of the fetch address, if the BTAC indicates that the fetch address hit in the BTAC and that the one of the plurality of target addresses is a valid target

address, and if the BTAC predicts that one of the plurality of branch instructions corresponding to the smallest the corresponding one of the plurality of offsets will be taken. The apparatus also includes address selection logic, coupled to the selector, which selects one of the plurality of target addresses as a subsequent fetch address for the instruction cache in response to the selector. The address selection logic selects the one of the plurality of target addresses as the subsequent fetch address for the instruction cache regardless of how many branch instructions are present in the instruction cache line selected by the fetch address.

In another aspect, it is a feature of the present invention to provide an apparatus for selecting a branch target address in a pipelined microprocessor having an instruction cache, a fetch address being provided to the instruction cache on an address bus selecting a line of instructions therein. The apparatus includes a branch target address cache (BTAC), coupled to the address bus, which provides information cached therein about a plurality of previously executed branch instructions indexed by the fetch address. The information includes a plurality of target addresses associated with the plurality of previously executed branch instructions. The apparatus also includes control logic, coupled to the BTAC, which selects as a subsequent fetch address on the address bus one of the plurality of target addresses associated with one of the plurality of branch instructions. The subsequent fetch address is selected in response to the information and the fetch address. The control logic selects the one of the plurality of target addresses that is valid, which is predicted taken, and that is first seen with respect to the fetch address. The one of the plurality of target addresses is selected whether or not a branch instruction is present in the line of instructions.

In another aspect, it is a feature of the present invention to provide a method for selecting a fetch address to provide to an instruction cache for speculatively branching a microprocessor. The method includes providing a plurality of target addresses and instruction cache line offsets of a corresponding plurality of previously executed branch instructions, in response to a first fetch address provided to the instruction cache. The method also includes providing a plurality of direction predictions. Each of the plurality of direction predictions predicts whether a corresponding one the plurality of previously

executed branch instructions will be taken. The method also includes providing a plurality of valid indications. Each of the plurality of valid indications indicates whether a corresponding one of the plurality of target addresses is a valid target address. The method also includes selecting one of the plurality of target addresses corresponding to one of the branch instructions that is valid, predicted taken, located after the first fetch address, and nearest the first fetch address as a second fetch address to provide to the instruction cache, in response to the providing the plurality of target addresses, instruction cache line offsets, direction predictions, and valid indications.

An advantage of the present invention is that provides a relatively fast way to select one of multiple cached branch instruction target addresses for a given instruction cache line using a relatively small amount of information about the branch instructions to be cached in the branch target address cache.

Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.

Please amend paragraph 87 on page 37 of the disclosure as follows:

The non-speculative branch direction predictor 412 generates a non-speculative prediction of the direction of a branch instruction 444, i.e., whether the branch will be taken or not taken, in response to the instruction decode information 492 received from the instruction decode logic 436. Preferably, the non-speculative branch direction predictor 412 includes one or more branch history tables for storing a history of resolved directions of executed branch instructions. Preferably, the branch history tables are used in conjunction with decode information of the branch instruction itself provided by the instruction decode logic 436 to predict a direction of conditional branch instructions. An exemplary embodiment of the non-speculative branch direction predictor 412 is described in U.S. Patent No. 6,550,004 entitled ~~application serial number 09/434,984 (Docket Number CNTR:1498)~~ HYBRID BRANCH PREDICTOR WITH IMPROVED SELECTOR TABLE UPDATE MECHANISM, having a common assignee and which is hereby incorporated by reference. Logic that ultimately resolves the direction of the branch instruction preferably resides in the E-stage 326 of the pipeline 300.

Please amend paragraph 90 on page 39 of the disclosure as follows:

An exemplary embodiment of the non-speculative call/return stack 414 is described in U.S. Patent No. 6,314,514 entitled ~~application serial number 09/271,591 (Docket Number CNTR:1500)~~ METHOD AND APPARATUS FOR CORRECTING AN INTERNAL CALL/RETURN STACK IN A MICROPROCESSOR THAT SPECULATIVELY EXECUTES CALL AND RETURN INSTRUCTIONS, having a common assignee and which is hereby incorporated by reference.

Please amend paragraph 91 on page 39 of the disclosure as follows:

The non-speculative target address calculator 416 generates the non-speculative target address 354 of Figure 3 in response to the instruction decode information 492 received from the instruction decode logic 436. Preferably, the non-speculative target address calculator 416 includes an arithmetic logic unit for calculating a branch target address of PC-relative or direct type branch instructions. Preferably, the arithmetic logic unit adds an instruction pointer and length of the branch instruction to a signed offset comprised in the branch instruction to calculate the target address of PC-relative type branch instructions. Preferably, the non-speculative target address calculator 416 includes a relatively small branch target buffer (BTB) for caching branch target addresses of indirect type branch instructions. An exemplary embodiment of the non-speculative target address calculator 416 is described in U.S. Patent No. 6,609,194 entitled ~~application serial number 09/438,907 (Docket Number CNTR:1507)~~ APPARATUS FOR PERFORMING BRANCH TARGET ADDRESS CALCULATION BASED ON BRANCH TYPE, having a common assignee and which is hereby incorporated by reference.